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Clean Version of Pending Claims

CIRCUITS WITH A TRENCH CAPACITOR HAVING MICRO-ROUGHENED SEMICONDUCTOR SURFACES
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Serial No.:09/467,992

Claims 17-19, 22-23, 26-27, 29, 31-51 as of January 10, 2002(date of response to first office action after CPA).

Sub F2 E1

17. (Twice Amended) A memory cell, comprising:

a transistor formed in a layer of semiconductor material outwardly from a substrate, the transistor including a first source/drain region, a body region and a second source/drain region;

a trench capacitor formed in a trench and coupled to the first source/drain region; and

a first plate of polycrystalline material formed in the trench that is coupled to a second plate integral with the first source/drain region thereby forming a conductorless electrical connection between the trench capacitor and the transistor, the second plate having an etch-roughened surface ; and

an insulator layer that separates the first polycrystalline plate from the etch-roughened surface of the second plate.

18. The memory cell of claim 17, wherein the first polycrystalline semiconductor plate comprises polysilicon.

19. The memory cell of claim 17, wherein the second plate comprises a heavily doped p-type silicon substrate.

22. A memory cell, comprising:

a vertical transistor formed outwardly from a substrate, the transistor including a first source/drain region, a body region and a second source/drain region that are vertically aligned;

wherein a surface of the first source/drain region includes integral therewith a first polycrystalline plate having a polycrystalline surface layer that is etch-roughened ;

a trench capacitor having a second plate that is formed in a trench that surrounds the first plate; and

wherein the first plate forms a conductorless electrical connection between the trench capacitor and the transistor.

23. The memory cell of claim 22, wherein the first plate integral with the first source/drain region comprises single crystalline silicon upon which is formed a layer of polysilicon .

26. A memory device, comprising:

an array of memory cells, each memory cell including an access transistor that is coupled to a trench capacitor wherein a first plate of the trench capacitor is integral with a first source/drain region so as to form a conductorless electrical connection between the trench capacitor and the access transistor, the first plate including a micro-roughened surface layer of porous polysilicon, and a second plate of the trench capacitor disposed adjacent to the first plate;

a number of bit lines that are each selectively coupled to a number of the memory cells at a second source/drain region of the access transistor;

a number of word lines disposed substantially orthogonal to the bit lines and coupled to gates of a number of access transistors; and

a row decoder coupled to the word lines and a column decoder coupled to the bit lines so as to selectively access the cells of the array.

27. The memory device of claim 26, wherein the first plate comprises a single crystalline layer upon which is formed the layer of polysilicon .

29. The memory device of claim 26, wherein the second plate comprises polysilicon.

31. (Twice Amended) A memory cell, comprising:

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a transistor formed in a layer of semiconductor material outwardly from a substrate, the transistor including a first source/drain region having a first plate formed integral therewith, a body region and a second source/drain region; and

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a trench capacitor formed in a trench and electrically coupled without an intervening conductor to the first plate;

wherein the trench capacitor includes a polysilicon plate formed in the trench that is coupled to the first plate of the first source/drain region, the first plate including a surface layer of polysilicon that is etch- roughened , and an insulator layer that separates the second polysilicon plate from the etch-roughened polysilicon surface of the first plate .

32. The memory cell of claim 31, wherein the first plate comprises heavily doped p-type silicon .

33. (Amended) A memory cell, comprising:

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a transistor formed in a layer of semiconductor material outwardly from a substrate, the transistor including a first source/drain region having a first plate formed integral therewith, a body region and a second source/drain region; and

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a trench capacitor formed in a trench and electrically coupled without an intervening conductor to the first plate;

wherein the trench capacitor includes a second plate of polysilicon formed in the trench so as to surround the first plate , and an insulator layer that separates the second polysilicon plate from at least the etch-roughened surface of the first plate.

34. A memory cell, comprising:

a vertical transistor formed outwardly from a substrate, the transistor including a first source/drain region, a body region and a second source/drain region that are vertically aligned, wherein the first source/drain region includes integral therewith a single crystalline silicon first plate with a layer of polysilicon having an etch-roughened surface; and

a trench capacitor with a second plate that is formed in a trench and that surrounds at least the etch-roughened surface of the first plate; and

wherein the first plate forms a conductorless electrical connection between the trench capacitor and the transistor.

35. A memory device, comprising:

an array of memory cells, each memory cell including an access transistor that is electrically connected without an intervening conductor to a trench capacitor by a first plate of the trench capacitor that is integral with a first source/drain region of the access transistor, the first plate including a micro-roughened surface of porous polysilicon , with a second plate of the trench capacitor disposed so as to surround at least the micro-roughened surface of the first plate;

a number of bit lines that are each selectively coupled to a number of the memory cells at a second source/drain region of the access transistor;

a number of word lines disposed substantially orthogonal to the bit lines and coupled to gates of a number of access transistors; and

a row decoder coupled to the word lines and a column decoder coupled to the bit lines so as to selectively access the cells of the array.

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36. (Twice Amended) The memory device of claim 35, wherein the access transistor includes a body region of p-type single crystalline silicon adjoining the first source/drain region, wherein the first source/drain region is n-type single crystalline silicon.

37. The memory cell of claim 31, wherein the first source/drain region is P-doped or N-doped.

38. The memory cell according to claim 33, wherein the first source/drain region is N-doped or P-doped.

39. The memory cell according to claim 34, wherein the single crystalline polysilicon is P-doped or N-doped.

40. The memory cell according to claim 35, wherein the first source/drain of the access transistor is P-doped or N-doped.

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41. (Twice Amended) A memory cell, comprising:

a transistor comprising outwardly from a substrate a first source/drain region at least a portion of which serves as a single crystalline first capacitor plate for forming a conductorless connection of the transistor to a trench capacitor, a body region and a second source/drain region, wherein the first capacitor plate includes a micro-roughened surface for increasing the capacitance of the trench capacitor;

the trench capacitor being formed in a trench surrounding a portion of the lateral transistor and including a second capacitor plate of polycrystalline material formed so as to surround the first capacitor; and

an insulator layer that separates the second polycrystalline semiconductor plate from the micro-roughened surface of the first plate.

42. A memory cell according to claim 41, wherein the micro-roughened surface of the first capacitor plate comprises a layer of polysilicon.

43. A memory cell according to claim 41, wherein the first source/drain that includes the first capacitor plate, the body region, and the second source/drain region are formed as a pillar of single-crystal semiconductor material.

44. A memory cell according to claim 41, wherein the second plate also surrounds first plates of adjacent memory cells.

45. A memory cell according to claim 44, wherein the second plate is grounded.

46. A memory cell according to claim 17, wherein the first plate also surrounds second plates of adjacent memory cells.

47. A memory cell according to claim 26, wherein the second plate also surrounds first plates of adjacent memory cells.

48. A memory cell according to claim 31, wherein the second plate also surrounds first plates of adjacent memory cells.

49. A memory cell according to claim 33, wherein the second plate also surrounds first plates of adjacent memory cells.

50. A memory cell according to claim 35, wherein the second plate also surrounds first plates of adjacent memory cells.

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51. (New) A memory cell comprising:

a lateral transistor formed in an upper portion of a single crystalline substrate and including a first source/drain region, a body region, and a second source/drain region;

a trench capacitor including a first plate formed by the substrate;

a trench formed in the substrate, the trench including a micro-roughened polysilicon surface, a second plate formed within the trench, and a dielectric layer separating the micro-roughed polysilicon trench surface from the second plate; and

a contact connecting the second source/drain region to the second plate.